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List of Abbreviations

Abbreviation	Denotation
5G	5th Generation
6G	6th Generation
AI	artificial intelligence
ASIC	application-specific integrated circuit
CN	core network
CPU	central processing unit
DNA	Deoxyribonucleic acid
DRAM	dynamic random-access memory
DSP	digital signal processing
EG	Expert Group
FPGA	field-programmable gate array
HW	hardware
IoT	internet of things
IP	intellectual property
ISA	instruction set architecture
KDT	key digital technologies
KPI	key performance indicator
MCM	multi-chip module
ML	machine learning
MPSoC	multiprocessor system on a chip
MRAM	magnetoresistive random-access memory
NVM	non-volatile memory
OEM	original equipment manufacturer
OS	operating system
R&I	research & innovation
RAN	radio access network
RoT	root of trust
SME	small and medium-sized enterprise
SNS	smart networks and services
SRAM	static random-access memory
SW	software
WP	Work package

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1 Introduction

COREnect (European Core Technologies for future connectivity systems and components) is a 2-year Coordination and Support Action project selected by the European Commission in the frame of the Horizon 2020 Research & Innovation programme, starting from 1st July 2020 [1].

Within 2 years of its duration, the COREnect will bring together the most prominent European industrial and academia players as well as industry associations in the network, microelectronics and verticals domains to jointly develop a high-level strategic roadmap of core subsystem and component technologies for supporting future connectivity. The goal is to establish a sustainable European technology sovereignty in 5th Generation (5G) and beyond, promote innovation and business opportunities e.g. for small and medium-sized enterprises (SMEs), pave the way for one or more future European champions in this area, and lay a solid foundation for the long-term success of both industries [2].

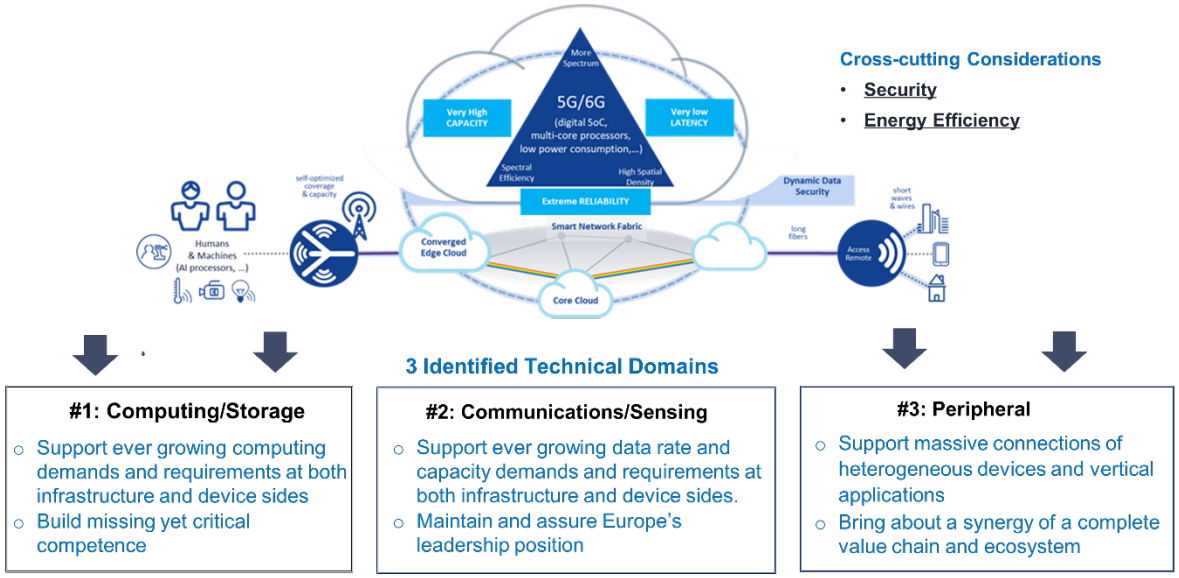

Figure 1: COREnect End-to-end System View and Scopes of Three Expert Groups

Based on the initially identified COREnect end-to-end system view together with value chain consideration as shown in Figure 1, COREnect organises three Expert Groups (EGs) within work package (WP) 3 to address industry roadmaps in three strategic focus areas

- Expert Group #1 Computing/Storage Core Technologies for Future network
- Expert Group #2 Communications/Sensing Core Technologies for Future network
- Expert Group #3 Peripheral Core Technologies for Future network

each of which consists of

- internal experts from COREnect technical partners (Bosch, Ericsson, III-V Lab/Nokia, TUD, Infineon, NXP, ST, IMEC, CEA)
- external experts identified by COREnect technical partners and community leaders (5G IA, AENEAS and AUSTRALO) as representing European research excellence on the topics.

The participations of all internal and external experts in COREnect are set on a voluntary basis without any payment. Potential refunding of travelling costs to attend Face-to-Face expert group meetings is foreseen if such meetings take place.

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The work of COREnect EGs kicked off on 1 October 2020 with a joint telco among the three EGs and is then organized within individual EGs. The chair/vice-chair(s) of each EG are responsible for the organization of its activities and interactions among experts via electronics tools such as emails, telco's and the digital collaboration platform features of MS Teams. A public workshop has been organized in conjunction with EFECS 2020 to discuss with key digital technologies (KDT) and smart network and services (SNS) communities [3].

This deliverable summarizes all the discussions and progress made in each EG during the period of October-December 2020, including scope, initially identified research areas and design considerations, meeting overviews and the planned next steps in 2021.

Following the top-down approach in COREnect, the work of EGs in WP3 is guided by WP2 that identifies potential technology gap on core component and subsystem technologies towards 6th Generation (6G) evolution and the research & innovation (R&I) areas where Europe should seize opportunities and strengthen its capabilities in the next 10 years. The discussion within each EG, among the 3 EGs as well as between WP2 and WP3 will continue in the project and will be captured and crystallized into D3.2 COREnect initial industry roadmap that is to be developed in the first half year of 2021.

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2 Expert Group 1 – Computing/Storage Core Technologies

2.1 Scope of Expert Group 1

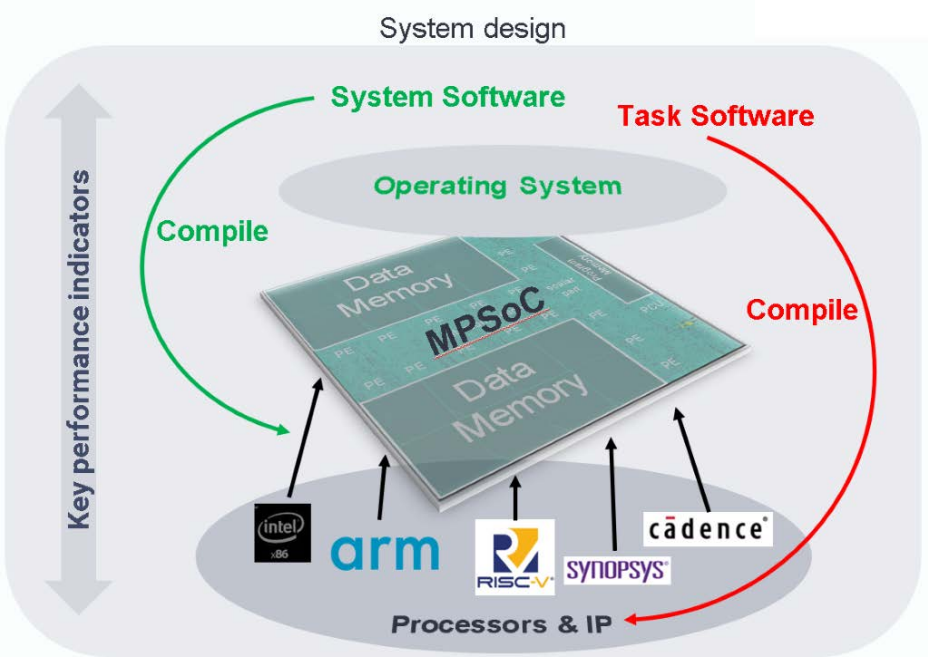

Figure 2: Common architecture of computing systems

Future connectivity systems and 6G will require ever more performant digital computing platforms and components. For those, Europe's dependence on outside suppliers is continuously increasing, especially after major European players have been acquired by outside companies. The goal of Expert Group 1 (EG1) is to identify open challenges for innovations in the area of digital computing chips that would ensure European technological sovereignty. Since controlling every component may not be realistic, EG1 will also analyze how to keep checks and balances.

When identifying these challenges, one needs to consider the communications architecture side of view and the applications side of view. The first requires an individual analysis of the electronics needed for terminals, the radio access network (RAN), and the core network (CN). From the applications side of view, the future applications of interest are the internet of things (IoT), personal devices and personal mobile robotics in the 2030s. For each of these applications, the different operating constraints as well as the need to support legacy software need to be considered.

In the scope of EG1, we propose the following research areas: first, to pinpoint the requirements for future digital computing systems, we present in subsection 2.2.1 a set of key performance indicators (KPIs) along which solutions in the following research areas have to measured. For the other research areas, we follow the common architecture that lies beneath the software stack from the bottom up, as illustrated in Figure 2: at the bottom there are processor cores, whose software interface is defined by the instruction set architecture (ISA), the topic of subsection 2.2.2. The core interacts with memory and storage, which gives us our third research area (c.f. subsection 2.2.3). Multiple cores, memories, and other intellectual property (IP) blocks are integrated in a multiprocessor system on a chip (MPSoC) or a multi-chip module (MCM). The associated challenges are described in subsection 2.2.4. On top of the MPSoC, an operating system (OS) runs, which provides the topmost abstraction layer, investigated in

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subsection 2.2.5. Finally, since these components are interconnected and need to be tailored to a specific function, we address the overall system architecture in subsection 2.2.6.

2.2 Initially Identified Research Areas and Design Considerations

2.2.1 Key performance indicators

One of the key elements of next-generation platforms for 5G/6G digital computing platforms is the fact that they need to operate in different working conditions or use cases, which will affect the target metrics or KPIs to consider for the optimal design. In particular, we can consider that such digital computing platforms will need to be implemented considering, at least, three different types of fundamental scenarios, namely:

- Scenario 1: mobile or portable smart devices (e.g., smartphones or laptops)
- Scenario 2: severely constrained devices (e.g., IoT objects, extreme edge sensors)
- Scenario 3: infrastructure equipment (e.g., access points, intermediate hubs or final base stations).

In all scenarios, the set of key performance indicators (KPIs) that need to be considered is multi-dimensional and includes energy, cost, performance, latency, real-time operation, safety, security, trustworthiness, sourcing level, compatibility, adaptability, and completeness of the software tooling to design and optimize the final system. The target values given to the KPIs for each scenario will be defined by EG1 contributors and will serve as inputs to estimate the gap in the key technologies addressed in this report.

Finally, an additional element to consider, which would affect how the KPIs can be achieved in the future is the nature of the considered electronic devices for the final designs. More precisely, for future devices, we need to consider that conventional digital circuits can be augmented with technologies from new computing paradigms such as neuromorphic circuits exploiting interesting analog properties of novel nanomaterials. Novel memories technologies such as Magnetoresistive random-access memories (MRAMs) or compute-in-memory and even Deoxyribonucleic acid (DNA) storage are likely to broaden the design choice in memory/storage. It is uncertain whether such emerging technologies will be available from the few (non-European controlled) foundries.

2.2.2 Instruction set architecture

The Instruction Set Architecture (ISA), can be seen as a contract between the hardware and software domain. It states the properties programmers can safely assume and functional behavior guaranteed by the engineers. As such, the ISA plays an integral part in any compute system but over the years the actual implementation has become more important than the ISA itself.

Where ISA and microprocessor often could be seen as two sides of the same medal, ARM dominates the mobile world without building physical chips. The ISA itself does not provide a competitive advantage in the market, as evidenced by virtually all Smartphones running on ARM. The microarchitecture, however, that is the design of the corresponding electronic circuits, is a critical competence as it forms the basis for building products and services. Being able to design and thus customize your own CPUs gives companies leverage over competitors who have to rely on software-only implementations.

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Although controlling an ISA is not sufficient, let alone necessary, for commercial success, its central role can be an enabling factor in boosting innovation. Recent years have exposed more and more shortcomings of established concepts:

- Growing importance of data processing algorithms that map poorly onto classic Von-Neumann style processor architectures
- Rising security awareness revealing inherent weaknesses when security is not a first-order concern
- Emerging Silicon technologies like persistent memories enabling radically new system architectures

2.2.3 Storage

Storage is a subset of memory hierarchies. The promise of an ideal memory hierarchy is to create an illusion that the memory system is as fast and energy-efficient as the top level (e.g., static random-access memory (SRAM)) and as inexpensive per gigabit and as high-capacity as the bottom level (e.g., rotating magnetic disk, optical storage, tape).

The underlying technology includes memory device physics, fabrication, memory array architecture, interfaces, packaging, memory controller design, ISA support, OS support, programming models.

System designers need to consider tradeoffs based on memory technology properties like endurance, density, cost per gigabit, latency and energy per read and write, bandwidth, reliability, sensitivity to security exploits (e.g., dynamic random-access memory (DRAM)'s row hammer).

High-speed connectivity (4G and up) has made remote storage practical. Instead of storing files locally on a device, they can be stored in a cloud, and read back/ streamed back at a finger tap, implementing the illusion that the device has the storage capacity of the cloud. Thus, it is important to remember that the network is part of the memory hierarchy.

We can expect that in the future the need for miniaturization and energy-efficiency of user devices will push further this partitioning between local and remote memory systems. For instance, local memory systems might be limited to cache subsystems highly integrated with embedded non-volatile memory (NVM), whereas remote memory systems might include a deep memory hierarchy, from caches to DRAM to storage-class memory and high-capacity storage. Local memory systems might utilize cheaper embedded memories using mature technology nodes, whereas remote memory systems might utilize expensive standalone memories using the latest technology nodes.

As technology scaling continues, Von Neumann architectures, that physically separate computation and memory, are becoming less relevant, especially for memory-centric applications. The need to minimize data transfer energy drives research areas like processing-in-memory, in-memory computing, near-memory computing: instead of moving data to compute, we can move compute to data (perform computation where it makes most sense). These research areas span both the digital and analog/mixed-signal domains. We should also consider NVM tightly coupled with SRAM-based in-memory computing to combine the advantages of both NVM and SRAM.

The following important questions should be considered in order to maintain or create European sovereignty. How to be or to become independent from main foundries located outside of Europe? How to deal with the market consolidation that has been reducing the number of foundries for decades and that will make Europe even more dependent on a unique supply chain? The following risks should be considered: a future disease pandemic would slow down even more this already long and unique supply

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chain; some country invading Taiwan would mean a loss of control over the TSMC major foundry; the exponential increase of silicon price might make research and confidential circuit design prohibitively expensive for Europe.

2.2.4 Multiprocessor system on a chip

The multiprocessor system on a chip (MPSoC) provides the hardware foundation of any computing platform. Recent innovations in processor design, interconnect and memory architectures show that a multitude of KPIs (c.f. subsection 2.2.1) can be met for selected application scenarios. However, many of today's MPSoCs lack to ensure trustworthiness to protect confidential data as well as to prevent attackers from compromising the whole system. For instance, MPSoCs must rely on untrusted third-party IP blocks to keep the design time within an acceptable range. This will inevitably introduce vulnerabilities and opens the system for attackers.

In the scope of EG1, we see the challenge in building a "Meta-level Fabric Architecture" for MPSoCs. There is a demand for a holistic view on several research questions:

- Ensure the isolation of MPSoC components including unknown and untrusted hardware (HW) blocks.
- Enable the secure and encrypted communication between these components.
- Verify the components to detect unusual behavior.
- Define the root of trust (RoT) as a tamper resistant security foundation of the MPSoC.

In summary, we want to understand the implications of such heterogeneous architectures and their tight connection towards OS and ISA keeping in mind the crosslinks to other KPIs. For example, the RoT provided on MPSoC level could replace vulnerable processor-intern units and OS-specific features such as memory management units or privilege levels, respectively.

2.2.5 Operating System

Referring to the KPIs as stated in subsection 2.2.1, the key challenges for an operating system (OS) are to:

- Concurrently run applications with diverse and potentially contradicting requirements at the same time on the same die/MPSoC. Example requirements are real-time (low jitter and low latency, almost deterministic execution), legacy support (e.g., Linux applications), high-security, etc.
- Accommodate HW/SW-IP of unknown origin and unclear trustworthiness (e.g., artificial intelligence (AI) accelerators, digital signal processing (DSP)s, field-programmable gate array (FPGA)) requiring novel approaches for isolation and protected communication
- Safety and reliability, i.e., provide basic means to tolerate failures of components so that degraded operation is possible (in non-safety-critical environment) or even guaranteed (in applications like autonomous driving); prevent kill-switch.
- Minimize power consumption.

We believe that state-of-the-art microkernel (µ-kernel)/hypervisor technology can form the base of the OS response to the challenges. This requires close interaction with ISA (for example to support virtual-

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ization and extremely efficient protection boundary crossing), MPSoC (to provide the basic space-encapsulation for untrusted HW/SW-IP, possibility for encrypted execution and establishment for root of trust), micro-architectures (to minimize interference), memory architectures (to support efficient virtualization, immediate start up), etc.

2.2.6 System architecture

The challenge of system architecture is *to find a form for a given function subject to given constraints and optimized for given objectives.* For 5G/6G systems, the starting point is a collection of 5G/6G functions, often called applications and or services.

From this perspective, the IISA, MPSoC, and OS, as described in earlier sections, are *form elements*. These define high-level interfaces that enable and promote the reuse of parts of the earlier system architecture. The *constraints* commonly are about adherence to standards, technologies, and legacy. The *objectives* identify optimization targets, and invariably include costs and power consumption.

Below a first (incomplete) attempt to list the *new* and *most critical* 5G/6G System Architecture challenges.

New function challenges:

- Scaling-up existing functions (e.g., higher resolution, lower latency), possibly leading to a 10x increase in compute and memory requirements. Up to 4G we could rely on the steady scaling of CMOS technology to support such an increase. However, for 5G/6G we need smarter, heterogenous architecture, with domain-specific accelerators (e.g., Convolutional neural network (CNN) accelerators).
- New functions/services (e.g., truly immersive X Reality (XR), high-fidelity mobile hologram, and digital twin [4]-[6]).

New form challenges:

- New ways of distributing the compute-loads and memory-needs of a function over the UE (user equipment), associated wearables, base station, the 5G/6G core, and the cloud. This is also known as the convergence of communications and computing.

New constraints:

- New architecture must address the concerns of end users relating to trust, privacy, and security. These are cross-cutting issues (all form elements, all system components), and in many respects lack accepted and workable definitions and standards.

New objectives:

- End-to-end latency must be reduced by at least 10x.

An overarching 5G/6G architecture challenge arises from the blurring of boundaries between historically distinct use cases and subsystems. For example, data centers and their virtual machines becoming part of the network itself, or network endpoints morphing from human interaction devices into autonomously operating devices.

2.3 Major Activities of Expert Group 1

2.3.1 Meeting Agenda and Summary

1st Expert Group 1 Meeting

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On November 3, EG1 had its first 1.5-hour meeting to initiate roadmapping work. The technical vision and strategy of COREnect were presented and possible research areas in the scope of EG1 were discussed. Here, ISA, MPSoC and OS were suggested as the first three main research areas, following the common foundation of a software stack. EG1 also defined a set of KPIs along which solutions in any of these areas have to be measured. Regarding the ISA, a consensus was reached that, while the importance of the single-core ISA has lessened in the last 20 years, providing efficient (c.f. aforementioned KPIs) implementations is still important. For MPSoCs, we identified the open challenge of defining a "meta-level fabric architecture". In regards to the OS, we decided to further investigate whether µ-kernels are the way forward to address future computing challenges. The results of the first meeting were presented in brief at the COREnect public workshop at EFECS [3].

2nd Expert Group 1 Meeting

In the second EG1 meeting on November 27, which was held in conjunction with EFECS, the discussion was continued and the audience feedback from EFECS was evaluated. As a result, EG1 has widened its scope to also include memory/storage, where traditional models are losing relevance, and overall system architecture, where one needs to find the right form for the specific function, instead of the other way around, as further research areas. It was also noted that for an OS to separate trusted components, it needs support from both, the MPSoC and the ISA (e.g., via an ISA extension for µ-kernels). The research areas were assigned to different experts for further research and for summary of the accomplished work.

2.3.2 Next Steps of Expert Group 1

In 2021, we want to invite more experts to participate in EG1. With the enhanced expertise, we want to review our initial research roadmap and concretize the suggestions made. To discuss this, we will have another workshop in conjunction with EuCNC in June 2021 along preliminary meetings before that. The result will be compiled in the next deliverable (D3.2).

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3 Expert Group 2 – Communications/Sensing Core Technologies

3.1 Scope of Expert Group 2

Expert group 2 (EG2) investigates how Europe can establish leadership and sovereignty in the field of communications and sensing. This field is subject to an insatiable demand for ever increasing data rates: future devices will have to process a huge amount of data with low latency, while more connected devices will drive the capacity and speed requirements for the infrastructure to unprecedented heights. Upcoming smart networks and communications systems will have to operate in an energy-efficient manner to allow massive use of AI and machine learning software for a decentralized network structure in which virtualization should enable a fluent flow of data that at the same time needs to be kept secure.

3.2 Initially Identified Research Areas and Design Considerations

The above scenario will be the outline for the development of future 6G systems by 2030. In the run up to 5G it is observed that Europe has lost weight in several parts of the connectivity supply chain. If this evolution continues, Europe might evolve to just a consumer market of foreign technology. This leaves very limited power to influence evolutions in connectivity in a world where technology is more and more seen as a source of geopolitical power. To act against this evolution, it is essential to first make an inventory of the most important research gaps in the field of communications and sensing.

As indicated in D2.1, it is expected that the gaps will differ over different areas within the field of communications and sensing. To enable such differentiation, four connectivity areas have been identified:

- Datacenter infrastructure for cloud centric applications
- Wireless infrastructure
- Industrial grade connectivity
- Consumer grade connectivity

During the first workshop of Expert Group 2 on November 28, 2020, these connectivity areas have been discussed with the experts. These areas were generally accepted and will form the basis for further analysis within this Expert Group. During this workshop, we also consulted the experts on their view on the key gaps in view of the European value chain and technological sovereignty, as explained below in Section 3.3. While a detailed processing of the inputs from experts is still ongoing, a few gaps have already been made clear. The gaps that have been identified most prominently are discussed in the subsections below. During further consultations and discussions with the experts during the COREnect project lifetime, these gaps with be further investigated and related call for actions will be identified.

3.2.1 Hardware design in very advanced CMOS

European foundries have stepped out of the More Moore scaling race. However, with advanced CMOS processing moved out of Europe, it is important that there is enough know-how on IC design in advanced CMOS. Indeed, in communications and sensing all functions are subject to more and more digitization (also fueled by AI and machine learning). As an illustration in the area of consumer grade connectivity, Europe does not have major fabless players like Qualcomm or Mediatek. Also, in the field of wireless

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infrastructure, the semiconductor content is increasing, calling again for IC design capabilities in advanced CMOS generations. Further, this gap comes together with the discussion on whether there should be a foundry for advanced CMOS processing on EU territory. This item concerns all expert groups and will be discussed further in the coming months.

3.2.2 Companies in the higher part of the value chain

Today, Europe delivers components, but it lacks connecting actors upwards the value chain. For example, in the field of consumer grade connectivity, Europe does not have an original equipment manufacturer (OEM) like Apple and, at an even higher level, no big companies like Google, Facebook, Microsoft and IBM that also dominate the cloud. Also, the absence of a processor company and a transceiver design company has been flagged by several experts.

3.2.3 Silicon photonics industry

In the area of datacenter infrastructure for cloud centric applications it is observed that there is no big player in Europe (anymore) on silicon photonics. Further, the design of high-speed application-specific integrated circuits (ASIC)s needed in this area has moved out of Europe.

3.2.4 Non-technical gaps

Several non-technical gaps have also been flagged such as insufficient access to Venture Capitalists for new companies and insufficient public funding in the fields where Europe is not dominating.

3.3 Major Activities of Expert Group 2

3.3.1 Meeting Agenda and Summary

The first Expert Group 2 meeting was an online meeting on November 28, 2020. This workshop was highly attended, as 41 experts attended from 25 different organization. The number of attendees were almost equally distributed over industry, research and academia. The goal of this meeting was to introduce the connectivity areas mentioned in the introduction of Section 3.2 and treat some open questions on the gaps and on European sovereignty. In order to allow all participants to give their inputs in a group as big as 40 participants, we organized an online brainstorm session based on sticky notes. This enabled and motivated all participants to participate to the discussion in a limited timeframe, independent on their vocality. In addition to that, this also allowed the experts to consult and get inspired based on each other's ideas/notes.

In this way, a sticky note brainstorm session has been organized first to let people identify themselves and situate themselves in along the value chain and connectivity areas. Based on the (anonymized) result below, it can be observed that participating experts are rather nicely distributed along the value chain. Note that we allowed the experts to add several notes if they are active in different locations in this value chain.

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Next, a gap analysis has been proposed first according to the four areas listed in the introduction of this section 3.2, after which participants had the opportunity to add extra areas. Here the area of edge computing devices has been identified by several participants.

In the last part of the meeting, four fundamental questions within the COREnect scope have been asked. The first two questions are related to the European value chain and the other questions are related to the European technological sovereignty:

1. What is missing to grow the European value chain coverage and how can this be realized?
2. What must be Europe's prime focus to strengthen its current leadership in the value chain and why? How can this be achieved?
3. From a strategic sovereignty point of view, what should be Europe-owned and why?
4. How to keep design capabilities while using technologies from non-European foundries?

Again, all experts provided their answers and opinions via brainstorm sessions using (online) sticky notes. These sessions were followed by an open discussion on the third question. Some of the key opinions of the participants to this question are summarized in the subsections of Section 3.2. More in-depth analyses of the expert's input will be performed in the coming weeks and will be reported in later reports.

3.3.2 Next Steps of Expert Group 2

The inputs given by the experts on the sticky notes brainstorms during the first workshop will be post-processed and ordered by the (vice-)chairs of EG2. Discussing the results of this action will be a main agenda point for the next EG2 meeting that is scheduled around February 2021.

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4 Expert Group 3 – Peripheral Core Technologies

4.1 Scope of Expert Group 3

In addition to computing and communications core technologies, future networks require the development of supplementary core technologies that support the design of computing components (EG1) and communications components (EG2) and are essential for controlling the telecommunication and vertical value chain. The goal of Expert Group 3 (EG3) is then to identify key challenges for innovations and sovereignty in the areas of peripheral core technologies for future network. This will encompass the following two key domains to focus upon:

- support massive connections of heterogeneous devices and vertical applications, especially for critical infrastructures
- bring about a synergy of a complete value chain and ecosystem for future connectivity systems.

For these domains, both technology and application requirements, as well as access to manufacturing and strategic choices of Europe in the value chain will be considered. As identified in D2.1, the key drivers within Europe lie in the areas of mobility, industrial IoT and personalized robotics, and connected society and industry.

In this context, three key areas of strategic importance are initially identified for the work of EG3 by the chair, vice-chair, and participating experts:

- Core Process Technologies for addressing the needs of Europe
- System and component architectures
- Power management and energy efficiency on device and system level

For each of these research areas we have identified a number of research topics to look into in more detail. In the next step, we will make a list of priority topics (must-haves) and a list of other topics (nice-to-haves) in each research area. For each research topic, we will evaluate what effort is needed to achieve it in Europe and in what timeframe that is feasible. Also, chair and vice-chair of EG3 will align selected topics with EG1 and EG2 by consultation of respective experts of the required field. The global goal of EG3 is to define the overall European strengths for maintaining and developing our strongholds in the domain of Peripheral Core Technologies. It targets to address selected weak points that are critical yet can be realistically achieved in Europe instead of a complete list where some of them are not feasible in realistic industry environment.

4.2 Initially Identified Research Areas and Design Considerations

4.2.1 Core Process/Enabler Technologies – what does Europe need?

Within this first area, the focus is on front-end and back-end manufacturing of connectivity components. Based on the discussion in EG3 so far, a list of research topics is initially identified. The key priorities in which we should identify the gaps and future solutions for Europe are:

- Heterogeneous integration (integrate circuits and antennas, 3D packaging, …)
- Split manufacturing and split foundry approach: what do in Europe and what do elsewhere, which areas we need to build a European sovereignty?

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- Design methodologies and tools as technology enablers

Other topics which require further discussion in EG3 are:

- How to build fully integrated systems and what is the role of Europe?
- How to secure the supply chain, how to overcome dependencies, how to handle sovereignty versus autarky?
- How to handle single packaging for converters, amplification and beamforming?
- Do we need to get assembly packaging back to Europe?
- What technologies to focus upon in Europe: RF-SOI, FD-SOI, CMOS, BiCMOS, RF-CMOS, GaN, InP, InP/Si, SiGe – where to further shrink down, what type of components to develop in these respective technologies?
- What strategy on beyond additive manufacturing, as this is very cost/time intensive for high-volume?
- What to do with higher frequencies and photonics, e.g., look into heterogeneous integration?

4.2.2 System and Component Architectures

The area of "System and Component Architectures" covers the architectures, design and tools of both systems and components. The key priorities which have been initially identified in the discussion of EG3 are:

- Safety, security, reliability, robustness, resilience and privacy: what to focus on and how to handle this and how can Europe set a standard on these?
- Edge sensing and edge computing, including AI and Machine Learning (ML)

Other topics which require further discussions in EG3 are:

- Distributed Architectures
- Seamless design methods and tools
- System validation
- Aggregation of data: layers of abstraction
- How to handle data anonymity?
- What about analog signal processing: sample or pre-processing, how to do more efficient, how to get smaller size?
- Do we need a CPU specific for communications?

4.2.3 Power Management

For this area, no priorities have been set yet. A number of topics will be addressed and discussed further in detail in the following months:

- How to build fully energy-efficient components?
- Elastic computing: reconfiguration in real-time
- Wake-up technologies
- Energy management of different energy sources
- Wireless energy transfer and energy harvesting
- Zero-power autonomous devices with no battery requirement

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4.3 Major Activities of Expert Group 3

4.3.1 Meeting Agenda and Summary

Before the 1st Expert Group Workshop, the Expert Group 3 conducted one internal meeting for a prior brainstorming with the experts as well as a general introduction with clarification of each expert's focus area. During that meeting, we discussed what is needed to obtain sovereignty in Europe with relation to peripherals and examined many challenges Europe needs to face. As a result, a first clustering was formed and shared on the collaboration platform for further feedback from the experts.

The first workshop was held on the 27th of November 2020, where we have further discussed, added and rearranged the clustering with 17 attendees. The results are three main research clusters, to which we are aligning concrete focus topics:

- *Core Process Technologies,*
- *System and Component Architectures,* and
- *Power Management.*

For the *Core Process Technologies*, we will discuss within EG3 how heterogeneous integration is of importance of efficient peripheral technologies as well as how split manufacturing is a promising technique to obtain Europe's sovereignty. Regarding the *System and Component Architectures*, key topics discussed in the industry roadmap are how Europe can focus on its strengths in safety, security, reliability, and privacy. In addition, we will also investigate technologies within EG3 like edge computing and sensing. In *Power Management*, open questions are how to cope with the increasing power demand of components and systems and obtain efficiency, e.g. with zero-power devices, wireless energy transfer, elastic computing, etc.

4.3.2 Next Steps of Expert Group 3

The EG3 Chair and Vice-Chair are further evaluating the inputs received during the workshop. The strategy for December is to gather further information in a direct exchange with experts and foster the collaboration on our work on MS Teams, the collaboration platform. There, the EG3 Chair and Vice-Chair are collecting further input from the experts, which now can assign themselves to a chapter and topic they are willing to contribute to. Else, we are also already defining the role of the reviewers, who will not directly be responsible for a chapter, but evaluate the content.

The next meeting with the experts will follow in January or February 2021 to get to the details of the matter – from the "what" to the "how".

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5 Conclusion

In this report, the three COREnect expert groups, Computing/Storage Core Technologies, Communications/Sensing Core Technologies as well as Peripheral Core Technologies presented their initial discussions on scope, initially identified research areas and design considerations, meeting overviews and the planned next steps in 2021.

In general, all the three EGs are committed to continue their collaboration with internal and external experts and WP2 for identifying and analysing R&I areas. An initial industry roadmap will be provided in the mid of 2021. In the next 6 months of the project, each EG plans to hold an independent expert group meeting in conjunction with EuCNC & 6G Summit 2021. A public workshop will be held at the same occasion jointly by the three EGs and other partners in the COREnect consortium. The exact dates and arrangements will be decided later based on the pandemic situation and available resources in the project. In addition, all the EGs will continue to work closely with partners in the COREnect consortium to enhance community awareness and interests, maximizing the social impact and influences of the project.

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Annex A: Organizational Statistics of CORENect Expert Groups

Expert Group 1 – Computing/Storage Core Technologies

Table 1 Roles of EG1 Management

Role	Name and Affiliation
EG Chair	Gerhard Fettweis (TUD)
EG Manager	Viktor Razilov (TUD)

Table 2 Numbers of Internal and External Experts from Industry, Research Institute and University domains

	Industry	Research Institute	University	Total
Internal	5	4	5	14
External	1	0	2	3
Total	6	4	7	17

Table 3 Numbers of Organizations that Experts affiliate with from Industry, Research Institute and University domains

	Industry	Research Institute	University	Total
Internal	3	3	1	7
External	1	0	2	3
Total	4	3	3	10

Expert Group 2 – Communications/Sensing Core Technologies

Table 4 Roles of EG2 Management

Role	Name and Affiliation
EG Chair	Piet Wambacq (IMEC)
EG Vice-Chair	Frederic Gianesello (ST)
EG Vice-Chair	Didier Belot (CEA)
EG Manager	Björn Debaillie (IMEC)

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Table 5 Numbers of Internal and External Experts from Industry, Research Institute and University domains

	Industry	Research Institute	University	Total
Internal	20	16	0	36
External	4	7	13	24
Total	24	23	13	60

Table 6 Numbers of Organizations that Experts affiliate with from Industry, Research Institute and University domains

	Industry	Research Institute	University	Total
Internal	7	2	0	9
External	3	8	12	23
Total	10	10	12	32

Expert Group 3 – Peripheral Core Technologies

Table 7 Roles of EG3 Management

Role	Name and Affiliation
EG Chair	Patrick Pype (NXP)
EG Vice-Chair	Jochen Koszescha (IFAG)
EG Manager	Marina Plietsch (IFAG)

Table 8 Numbers of Internal and External Experts from Industry, Research Institute and University domains

	Industry	Research Institute	University	Other	Total
Internal	8	1	0		9
External	2	2	4	1	8
Total	10	3	4		17

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Table 9 Numbers of Organizations that Experts affiliate with from Industry, Research Institute and University domains

	Industry	Research Institute	University	Other	Total
Internal	5	1	0		6
External	2	1	4	1	8
Total	7	2	4	1	14

References

[1] https://cordis.europa.eu/project/id/956830

[2] https://www.corenect.eu/

[3] https://efecs.eu/co-located-workshops.html

[4] Ericsson, Whitepaper on Ever-present intelligent communication, 2020, https://www.ericsson.com/en/reports-and-papers/white-papers/a-research-outlook-towards-6g

[5] Nokia Bell-lab, Whitepaper on Communications in the Era of 6G, 2020, https://onestore.nokia.com/asset/207766

[6] https://cdn.codeground.org/nsr/downloads/researchareas/6G%20Vision.pdf

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